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A Novel Zero-Voltage-Switching Pwm Full Bridge Converter with Reduced Distortions

[1,]S. Moodasir Basha,[2,] S.Suresh , [3,]N.Vijaya Simha
[1,]*Assistant professor CRE college Tirupathi,*
[2,]*PG Scholar KEC,*
[3,]*Assistant professor CRE college Tirupathi*

ABSTRACT: Introducing resonant inductance and clamping diodes into the full-bridge converter can eliminate the voltage oscillation across the rectifier diodes and increase the load range for zero-voltage-switching (ZVS) achievement. The resonant inductance is shorted and its current keeps constant when the clamping diode is conducting, and the clamping diode is hard turned-off, causing significant reverse recovery loss if the output filter inductance is relatively larger. This paper improves the full-bridge converter by introducing a reset winding in series with the resonant inductance to make the clamping diode current decay rapidly when it conducts. The reset winding not only reduces the conduction losses, but also makes the clamping diodes naturally turn-off and avoids the reverse recovery. As the diodes are turn off naturally and reverse recovery voltage is avoided the distortions caused in the output voltage is removed to a maximum extend by varying the turns ratio of the transformer the energy stored in the reset winding is also increased by which the inductor value of the snubber circuit to turn off the clamping diodes also increases, which results in reductions in the distortions of the output voltage. The operation principle of the proposed converter is analyzed. The design of the turns ratio of transformer is discussed. A 1 kW prototype converter is built to verify the operation principle and the experimental results are also demonstrated.

I. INTRODUCTION

The full-bridge converter is widely used in medium-to-high power dc–dc conversions because it can achieve soft-switching without adding any auxiliary switches. The soft-switching techniques for PWM full bridge converter can be classified into two kinds: one is zero-voltage-switching and the other is zero-voltage and zero-current-switching.The leakage inductance of the transformer and the intrinsic capacitors of the switches are used to achieve ZVS for the switches. The ZVS characteristics are load dependent and will be lost at light load In ZVZCS PWM full-bridge converters, one leg achieves ZVS, and the other leg achieves ZCS .However, there is serious voltage oscillation across the rectifier diodes caused by the reverse recovery no matter ZVS or ZVZCS is realized for the switches. In order to overcome this problem, introduce a resonant inductance and two clamping diodes into the primary side of transformer. The solution eliminates the voltage ringing and overshoot, thus the voltage stress of the rectifier diodes is reduced, and without introducing losses or an additional controlled power device. The difference between the two locations of the resonant inductance and the transformer was analyzed and an optimal position was presented analyzed the issue in detail and also observed the effects of the blocking capacitor in different positions, and a best scheme was determined. No matter what the positions of the transformer and the resonant inductance are, the resonant inductance is clamped and its current keeps constant when the clamping diodes conduct. The output filter inductance must had enough current ripple so that the clamping diodes turn off naturally, otherwise the clamping diodes will be forced to be turned off, resulting in serious reverse recovery. In this paper, an auxiliary transformer winding is introduced to the ZVS PWM full-bridge converter to be in series with the resonant inductance. The introduced winding not only makes the clamping diode current decay rapidly and reduces the primary side conduction losses, but also can makes the current ripple of the output filter be smaller; hence the output filter capacitor can be reduced. The winding plays the role of forcing the clamping diode current to decay to zero, so it is called reset winding.

II. OPERATION PRINCIPLE

The proposed ZVS PWM full-bridge converter with reset winding is shown in Fig. 2.6, where the introduced is reset winding. The popular phase-shifted control is used for the converter where and form the leading leg and form the lagging leg. The converters are defined as type and type, respectively, since the primary winding is connected with the lagging leg and the leading leg, respectively.

The operation principle of the two types is similar and the difference is the same as described i.e., the clamping diodes conduct only once in type while conduct twice in type. The following description will be focused on the type. The key waveforms of the ZVS PWM full-bridge converter with/without reset winding are shown in. The full-bridge converter without reset winding was analyzed in detail, so the operation principle of the converter with reset winding is analyzed as follows:

A) All the switches and diodes are ideal, except for the rectifier diode, which is equivalent to an ideal diode and a paralleled capacitor to simulate the reverse recovery.
B) All the capacitors, inductance and transformer are ideal.
C) The turns ratio of the transformer is the primary winding: the reset winding: the secondary winding shows the equivalent circuits of the switching stages in a half period. The second half period is similar to the first half period.

[1] Prior to, the power is transferred from the input source to the load through and is turned off at zero voltage due to and limit the rising rate of the voltage across . The resonant inductance current charges and discharges, and the potential voltage of point decays. In the meanwhile, the capacitor is discharged. As the potential voltage of point is greater than zero, is reverse biased. The voltage of decreases to zero at and conducts naturally.

[2] 2.Can be turned on at zero voltage when conducts. Continues to be discharged since the voltage of point is still higher than zero. And continue decaying. This stage finishes when and the voltage of point reduces to zero correspondingly.

[3] 3.Conduct simultaneously, clamping the secondary voltage at zero. Is equal to and the circuit Operates in free-wheeling mode.

[4] 4.Conducts naturally when decays to zero, and can be turned on at zero voltage. To simpof them decay linearly with the rate of. At and cross zero, and continue increasing linearly in the negative direction. The load current flows through both the rectifier diodes. At and reach the reflected filter inductance current, and turn off.

[5] 5.Resonates with after, and is charged in a resonant manner. And continue increasing. At the voltage of rises to 2, and the primary voltage of the transformer, is, the potential voltage of point reduces to zero. So conducts, clamping at, and the voltage of is clamped at 2 accordingly. Declines downwards to the reflected filter inductance current when conducts, and increases in the negative direction. The voltage of the reset winding is, which is applied to making decrease quickly is greater than before and the current difference flows through this stage finishes when equals at and turns off naturally.

III. MAIN CIRCUIT

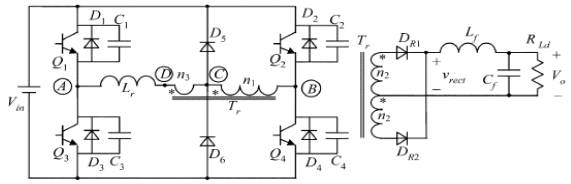


Fig.3.1.(A)

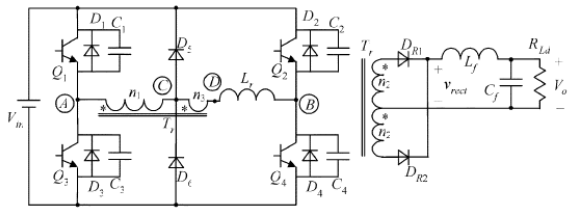


Fig.3.1.(b)

The proposed ZVS PWM full-bridge converter with reset winding is shown in Fig.3.1, where n3 is the introduced reset winding. The popular phase-shifted control is used for the converter where Q1and Q3 form the leading leg and Q2 and Q4 form the lagging leg. The converters in Fig.3. 1(a) and (b) are defined as Tr_lag type and Tr_leag type, respectively, since the primary winding(n1) is connected with the lagging leg and the leading leg, respectively. The operation principle of the two types is similar and the difference is the same as described

in the clamping diodes conduct only once in Tr_lag type while conduct twice in Tr_lead type. The following description will be focused on the Tr_lag type. The operation principle of the converter with reset winding is analyzed as follows.

To simplify the analysis, the following assumptions are made.

1) All the switches and diodes are ideal, except for the rectifier diode, which is equivalent to an ideal diode and a paralleled capacitor to simulate the reverse recovery.
2) All the capacitors, inductance and transformer are ideal.
3) The turn's ratio of the transformer is the primary winding: the reset winding: the secondary winding =n1:n2:n3.

1) Stage 1

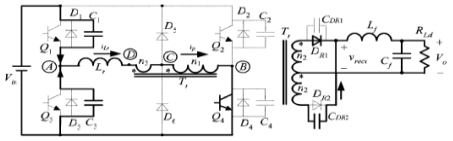


Fig. 3(a)

Prior to , the power is transferred from the input source Vin to the load through Q1,Q4 and Dr1.Q1 is turned off at zero voltage due to C1andC3 limit the rising rate of the voltage across Q1. The resonant inductance current iLr charges C1 and discharges C3 , and the potential voltage of point A decays. In the meanwhile, the capacitor Cdr2 is discharged. As the potential voltage of point Cis greater than zero, D6is reverse biased. The voltage of C3 decreases to zero at t1 and D3 conducts naturally.

2) Stage 2

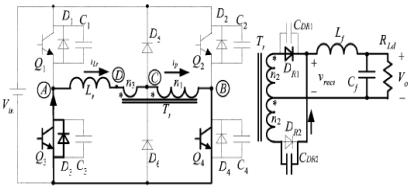


Fig. 3(b)

Q3 can be turned on at zero voltage when D3 conducts. Cdr2 continues to be discharged since the voltage of point is still higher than zero. iLr and ip continue decaying. This stage finishes when vcdr2=0 and the voltage of Point C reduce to zero correspondingly.

3) Stage 3

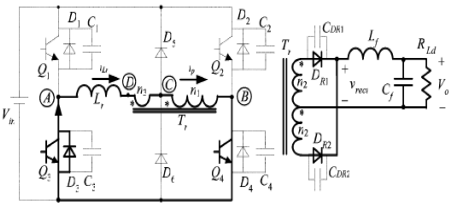


Fig. 3(c)

Dr1and Dr2 conduct simultaneously, clamping the secondary voltage at zero.iLr is equal to ip , and the circuit operates in free-wheeling mode.

4) Stage 4

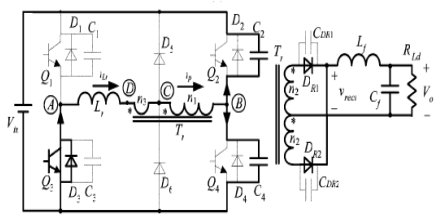


Fig. 3(d)

Q4 is turned off at zero voltage at t3, and C4 is charged and C2 is discharged in a resonant manner. This stage finishes when VC4 rises to Vin and VC2 falls to zero at t4 .

5) Stage 5

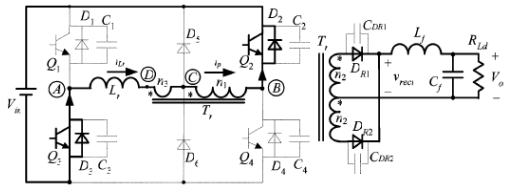


Fig. 3(e)

D2 conducts naturally when VC2 decays to zero, and Q2 can be turned on at zero voltage. iLr is equal to ip , and both of them decay linearly with the rate of Vin/Lr . At t5,iLr and ip cross zero, and continue increasing linearly in the negative direction. The load current flows through both the rectifier diodes. At t6 iLr and ip reach the reflected filter inductance current, and DR1 turns off.

1) **Stage 6**

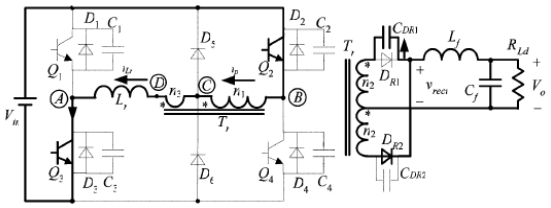


Fig. 3(f)

Lr resonates with CDR1 after t6 , and CDR1 is charged in a resonant manner. Ip and iLr continue increasing. At t7, the voltage of CDR1 rises to 2 Vin.n2/n1, and the primary voltage of the transformer, VBC, is Vin , the potential voltage of point C reduces to zero. So D6 conducts, clamping VBC at Vin , and the voltage of CDR1 is clamped at 2 Vin.n2/n1 accordingly.

7) Stage 7

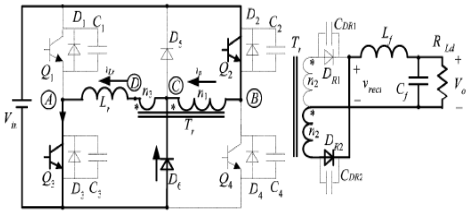


Fig. 3(g)

ip declines downwards to the reflected filter inductance current when D6 conducts, and increases in the negative direction. The voltage of the reset winding is Vin.n3/n1, which is applied to Lr , making iLr decrease quickly. iLr is greater than |ip| before t8 , and the current difference flows through D6. This stage finishes when ip equals iLr at t8 , and D6 turns off naturally. The further simplified equivalent circuit of this stage is shown in Fig. 4(a).

8) Stage 8

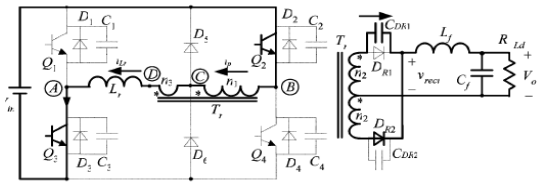


Fig. 3(h)

The reset winding is in series with the primary winding after D6 turns off, the further simplified equivalent circuit of this stage is shown in Fig. 4(b). During this stage, Lr resonates with CDR1. The rectifier voltage Vrect is given by

$$v_{\text{rect}}(t) = \frac{n_2}{n_1 + n_3} V_{\text{in}} + \left(\frac{n_2}{n_1} - \frac{n_2}{n_1 + n_3}\right) V_{\text{in}} \cos \omega (t - t_8) \quad (1)$$

where $\omega = 1/\sqrt{L_r \cdot C'_D}$, and $C'_D = C_{\text{DR1}}[2n_2/(n_1 + n_3)]^2$.

Equation (1) illustrates that the maximum value of Vrect will never exceed Vin.n2/n1 though slight oscillation exists. In practice, Vrect will finally stay at the average value Vin.n2/(n1+n3) since the inherent parasitic resistance exists in the power circuit.

IV. EQUIVALENT CIRCUIT

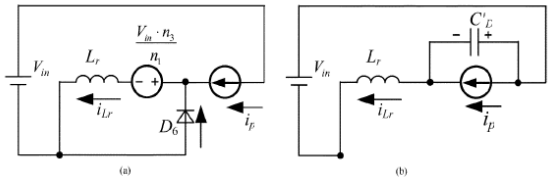


Fig. 3(i)

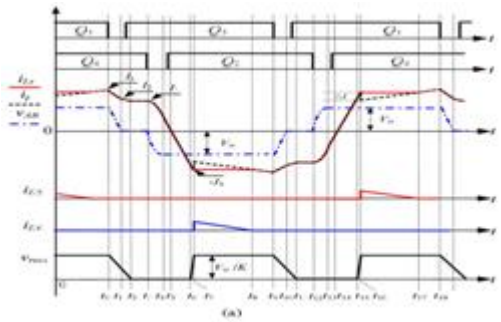


Fig3.6.a

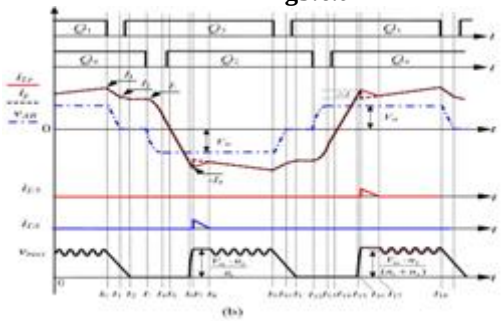


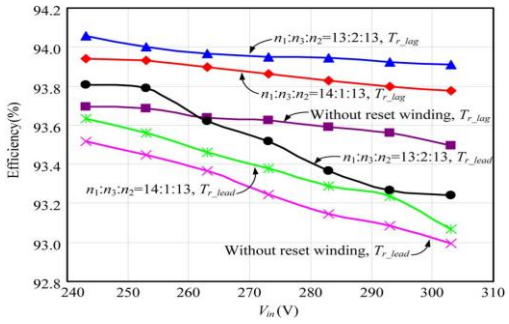
Fig3.6.b

IV EXPERIMENTAL VERIFICATION

A prototype with 180V/6A output of the proposed ZVS PWM full-bridge converter was built and tested to verify the operation principle. The output filter inductance is 230 H. Three kinds of transformer are built with different turn's ratio and their winding structures. All the transformers are built with the same core, bobbin and the size of the winding. It can be seen that the winding structures of three transformers are the same, and the only difference is the primary winding is split into two windings and a connecting port is added in the proposed converter. Hence, there is almost no extra cost and labor compared with traditional transformer.

The waveforms at full load under the nominal input voltage 270 V. Fig.2.6 shows the waveforms of the converter without reset winding the waveforms of the proposed type converter. With turns ration and 14:1:13, respectively. It can be seen that the clamping diode conduction time is shortened when the reset winding is added and the larger is, the shorter conduction time is. As the conduction time is shortened, the clamping diode

current is reduced, leading to a low conduction loss. The waveform of has slight oscillation after the clamping diodes turn off, however, the maximum value never exceed. Show the waveforms of the gate-source voltage, the drain-source voltage and the drain current of and, respectively. It can be seen that all switches realize ZVS. The waveforms of type converters [include the conventional full-bridge converter and the proposed type. It can be seen that the clamping diodes conduct twice in a switching period comparing with that of the type converters and the other waveforms are almost the same.



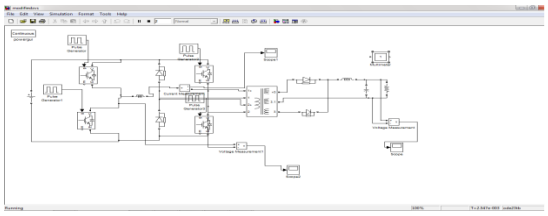
V. SUMILATION RESULTS

The circuit simulation for the elementary circuits of the a Novel Zero-Voltage-Switching PWM Full bridge Converter with Reduced Distortions is performed using MATLAB software

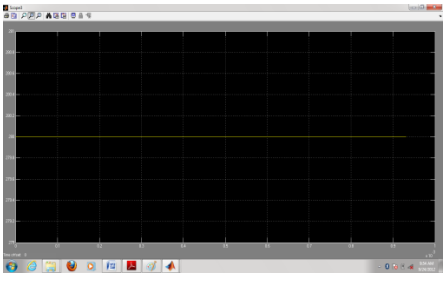
Elementary Circuit Design

Input voltage Vin=270
Filter Inductor Lf=8.5u H
Filter Capacitor Cf=600 p F
Switching Frequency Fs=10 M Hz
Transformer turns ratio n1:n2:n3=14:1:13
Maximum output voltage Vo=180 VDC
Duty cycle=44

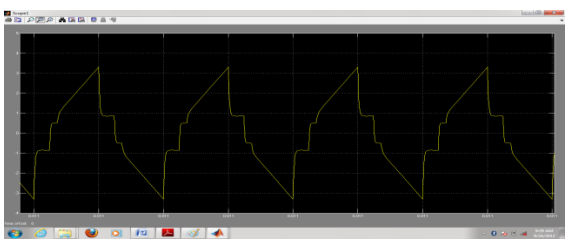
SIMULATAION CIRCUIT



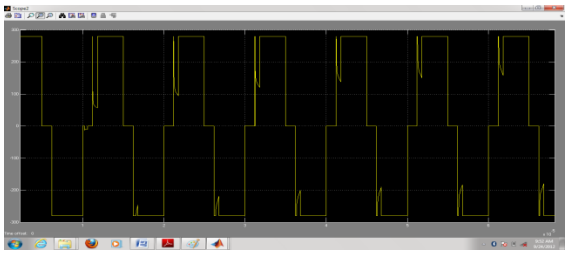
INPUT VOLTAGE



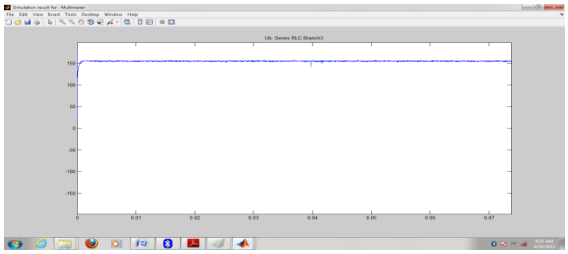
INDUCTOR CURRENT



RECTIFIER OUTPUT VOLTAGE



OUTPUT VOLTAGE



VI. CONCLUSION

A new ZVS PWM full-bridge converter is proposed in this paper, it employs an additional reset winding to make the clamping diode current decay rapidly when the clamping diode conducts, thus the conduction losses of the clamping diodes, the leading switches and the resonant inductance are reduced and the conversion efficiency can be increased. In the meanwhile, the clamping diodes can be turned off naturally without reverse recovery over the whole input voltage range, and the output filter inductance can be designed to be large to obtain small current ripple, leading to reduced filter capacitance. Compared with the traditional full bridge converter the proposed circuit provides another simple and effective approach to avoid the reverse recovery of the clamping diodes. The operation principle features and comparisons are illustrated. The Experimental results from the prototype are shown to verify the feasibility of the proposed converter

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[17] X. Ruan and F. Liu, "An improved zvs pwm full-bridge converter with clamping diodes," in *Proc. IEEE Power Electron. Spec. Conf. (PESC'04)*, 2004, pp. 1476–1481. **Wu Chen** (S'05) was born in Jiangsu, China, in 1981. He received the B.S. and M.S. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2003 and 2006, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering. His main research interests are soft-switching dc–dc converters and power electronics system integration.