

Cntfet Technology Based Precision Full-Wave Rectifier Using Ddcc

¹Gavendra Singh, ²Umesh Kumar, ³Rajeev Ranjan
^{1, 2, 3}(Student, Delhi Technological University, Delhi)

Abstract -This paper is the HSPICE implementation of 32nm CNTFET technology based rectifier using DDCC (differential difference current conveyor). The circuit proposes low design complexity, high temperature stability, larger bandwidth of operation and higher packaging density. The circuit also offers high input impedance and lower output impedance. Simulation result shows the performance of the circuit design validity.

Keywords – CMOS, CNTFET, DDCC, HSPICE, rectifier,

I. INTRODUCTION

Full-wave rectifier is used in RF demodulator, piecewise linear function generator, AC voltmeter, watt meter, and various nonlinear analog signal processing circuits[9]. A typical rectifier realized by using diodes, cannot rectify signals whose amplitudes are less than the threshold voltage(approximately 0.7V for silicon diode and approximately 0.3 for germanium diode).As a result diode-only rectifiers are used in only those applications in which the precision in the range of threshold voltage is insignificant, such as RF demodulators and DC voltage supply rectifiers, but for applications requiring accuracy the range of threshold voltage the diode-only rectifier cannot be used be used. This can be overcome by using integrated circuit rectifiers instead. The precision rectifiers based on operational amplifier (op-amp), diodes and resistors are presented. However, the classical problem with conventional precision rectifiers based on op-amps and diodes is that during the no conduction / conduction transition of the diodes, the op-amps must recover with a finite small-signal[9][10], dv/dt, (slew-rate) resulting in significant distortion during the zero crossing of the input signal. The use of the high slew-rate op-amps does not solve this problem because it is a small signal transient problem. The gain-band width is a parameter of op-amp that limits the high frequency performance of this scheme. Moreover, since these structures use the op-amp and the resistors, it is not suitable for IC fabrication. The proposed full-wave rectifier circuit shows better precision.

In the previous works on DDCC[7] with CMOS (350nm), the circuits suffer from the problem of leakage current. Also, the design was having lower packaging density. Current-mode circuits have always been a better choice for accuracy and high frequency performances. Differential difference current conveyor (DDCC) can be counted as the combination of CCII and DDA (differential difference amplifier) with their advantages[7][9]. The DDCC implementation with carbon nanotube field effect transistor shows better high frequency performance.



Fig.1- symbol for nCNTFET (a) and pCNTFET (b)

The proposed CNTFET[2][3] features large and small signal application, a compact model of intrinsic channel[2] region of MOSFET-like single-walled carbon nanotube[1] FET. We project a 13 times CV/I improvement of the intrinsic CNTFET with (19, 0) CNT over the bulk n-type MOSFET at the 32-nm node. The electrical symbols of nCNTFET and pCNTFET are shown in fig-1.

The rest of the paper is organized as follows. The section-II will be consisting of the carbon nanotube field effect transistor basic introduction with design parameters[1] and device response implementation in HSPICE. In the section-III we shall go for the basics of differential difference current conveyor(DDCC) and its performance comparison when CMOS and CNTFET technologies are used to design it(DDCC). In the section-IV, we shall go for the design of precision full-wave rectifier using CNTFET based DDCC.

II. CNTFET TECHNOLOGY

The six-capacitor model[2][3] is shown fig.-2, assuming that all the carriers from +k branches[2] are assigned to the source and that all the carriers from -k branches[2] are assigned to the drain. The I-V characteristics of the CNTFET are shown in Fig. 3, and they are similar to those of MOSFET. The CNTFET device current is saturated at higher V_{ds} (drain-to-source voltage) as shown in Fig. 2, and the ON-current decreases due to energy quantization in the axial direction at 32 nm (or less) gate length. The threshold voltage is defined as the voltage required to turn on the transistor, and the threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap, which is an inverse function of the diameter mentioned in equ.1.

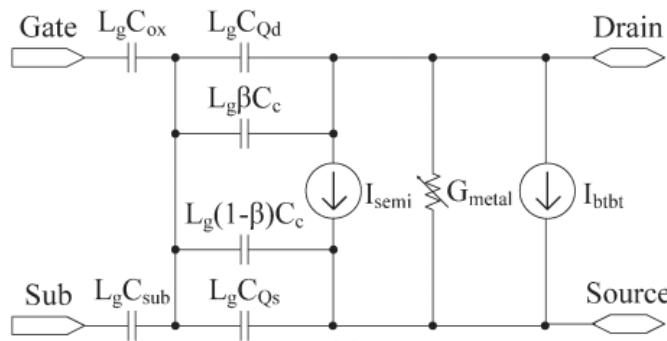


Fig 2- Six-capacitor equivalent model of CNTFET

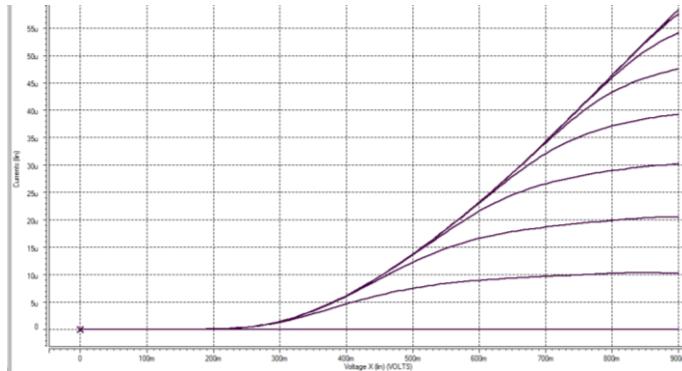


Fig3- Transfer characteristics of nCNTFET transistor

$$V_{th} \approx \frac{Eg}{2e} = \frac{\sqrt{3}}{3} \frac{aV_\pi}{eD_{CNT}} \quad (1)$$

where $a = 2.49 \text{ \AA}$ is the carbon-to-carbon atom distance, $V_\pi = 3.033 \text{ eV}$ is the carbon $\pi-\pi$ bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter. Then, the threshold voltage of the CNTFETs using (19, 0) CNTs[1] as channels is 0.289 V because D_{CNT} of a (19, 0) CNT is 1.49 nm. Simulation results have confirmed the correctness of this threshold voltage. Parameters for design are specified as follows:

```

q=1.60e-19      $ Electronic charge
Vpi=3.033       $ The carbon PI-PI bond energy
d=0.144e-9      $ The carbon PI-PI bond distance
a=0.2495e-9     $ The carbon atom distance
pi=3.1416        $ PI, constant
h=6.63e-14       $ Planck constant,X1e20
h_ba=1.0552e-14 $ h_bar, X1e20
k=8.617e-5       $ Boltzmann constant
epso=8.85e-12    $ Dielectric constant in vacuum
Cgsub=30e-12     $ Metal gate (W) to Substrate fringe capacitance per unit length, approximated as
                  30af/um, with 10um thick SiO2 default 30e-12
Cgabove=27e-12   $ W local interconnect to M1 coupling capacitance, 500nm apart, infinite large plane
                  default 27e-12
Cc_cnt=26e-12    $ The coupling capacitance between CNTs with 2Fs=6.4nm, about 26pF/m
Ccabove=15e-12   $ Coupling capacitance between CNT and the above M1 layer, 500nm apart, default
                  15e-12
Cc_gate=78e-12   $ The coupling capacitance between gates with 2F=64nm, about 78pF/m, W=32nm,
                  H=64nm, contact spacing 32nm default 78e-12
Ctot='Cgsub+Cgabove+Cc_gate+Cc_gate' $ total coupling capacitance for gate region
Lceff=200e-9      $ The mean free path in intrinsic CNT, estimated as 200nm
phi_M=4.5         $ Metal work function default=4.6
phi_S=4.5         $ CNT work function

```

III. THE DDCC DEVICE

The electrical symbol of DDCC[8] is shown in Fig-3(a). It has three voltage input terminals: Y1, Y2 and Y3, which have high input impedance. Terminal X is a low impedance current input terminal. There is a high impedance current output terminal Z. . The input-output characteristics of ideal DDCC are described in fig-3(b).

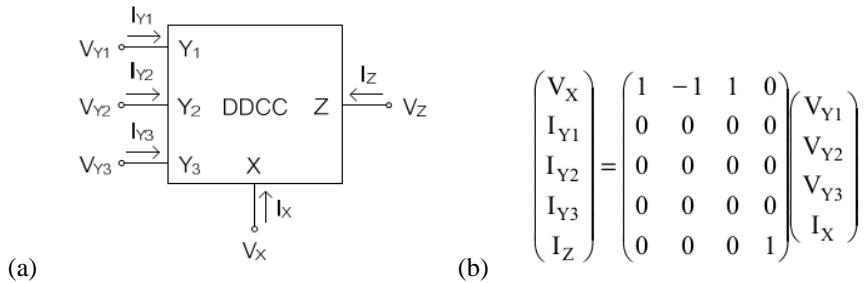


Fig 3. DDCC circuit symbol(a) and characteristics(b)

the circuit diagram for the DDCC device(CNTFET Technology based) is shown in fig-4 where pCNTFET and nCNTFET can be replace by pMOS and nMOS respectivily for MOS based device implentation.

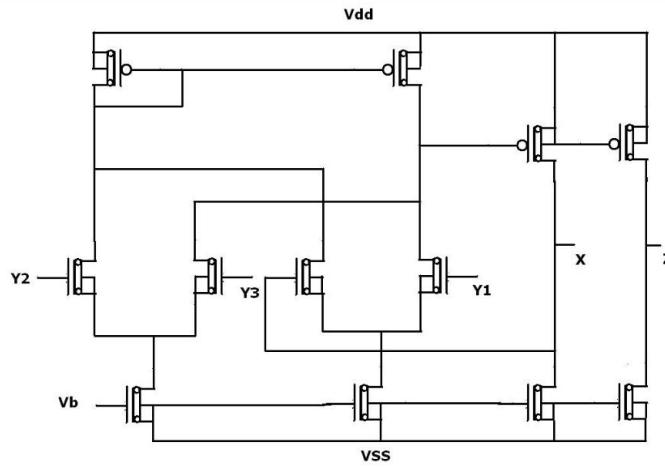


Fig4- circuit diagram of DDCC

The characteristics of the DDCC device can be view in fig.-5 where V_x vs. V_y1 has been indicated with parametric analysis with respect to V_{y2} .

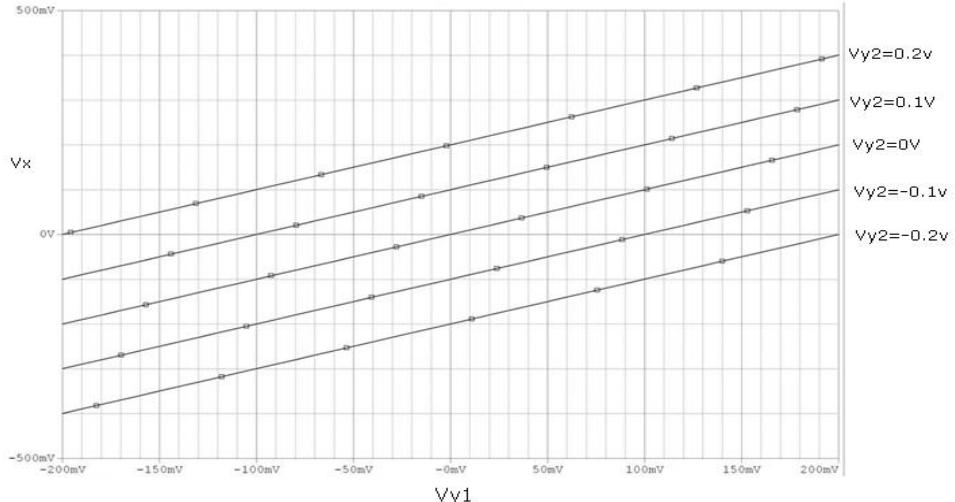


Fig. 5- Input-output characteristics of DDCC

The ciruit realization in HSPICE[2][3] can be done with following program:

```
.TITLE 'ddcc_CNFET'
*****
*For optimal accuracy, convergence, and runtime
*****
.options POST
.options AUTOSTOP
.options INGOLD=2 DCON=1
.options GSHUNT=1e-12 RMIN=1e-15
.options ABSTOL=1e-5 ABSVDC=1e-4
.options RELTOL=1e-2 RELVDC=1e-2
.options NUMDGT=4 PIVOT=13

.param TEMP=27
*****
*Include relevant model files
*****
```

```

.lib 'CNFET.lib' CNFET
*****
*Beginning of circuit and device definitions
*****

*Some CNFET parameters:
.param Ccsd=0 CoupleRatio=0
.param m_cnt=1 Efo=0.6
.param Wg=0 Cb=40e-12
.param Lg=32e-9 Lgef=100e-9
.param Vfn=0 Vfp=0
.param m=19 n=0
.param Hox=4e-9 Kox=16

*****
* Define power supply
*****
*DUMMY VOLTAGE SOURCE
*V1 11 0 DC 0.3V
v2 5 0 dc 0V
v3 8 0 dc 0V
vb 6 0 dc -0.7V

*sin voltage sources for transient analysis
V1 11 0 sin 0 0.2V 1khz
*V2 5 0 sin 0 0.3V 1khz
*V3 6 0 sin 0 0.3V 1khz

*ac source for ac sweep analysis
*V1 11 0 ac 0.2V

* APPLIED VOLTAGE
VDD 1 0 DC 0.9V
VSS 0 2 DC 0.9V

*****
* Main Circuits
*****



M1 4 5 7 7 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M2 9 8 7 7 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M3 4 12 10 10 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M4 9 11 10 10 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M5 4 4 1 1 PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M6 9 4 1 1 PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M7 12 9 1 1 PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9

```

+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M8 13 9 1 1 PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9

+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M9 7 6 2 2 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9

+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M10 10 6 2 2 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9

+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M11 12 6 2 2 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9

+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

M12 13 6 2 2 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9

+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

*.DC V2 -0.3 0.3 0.001

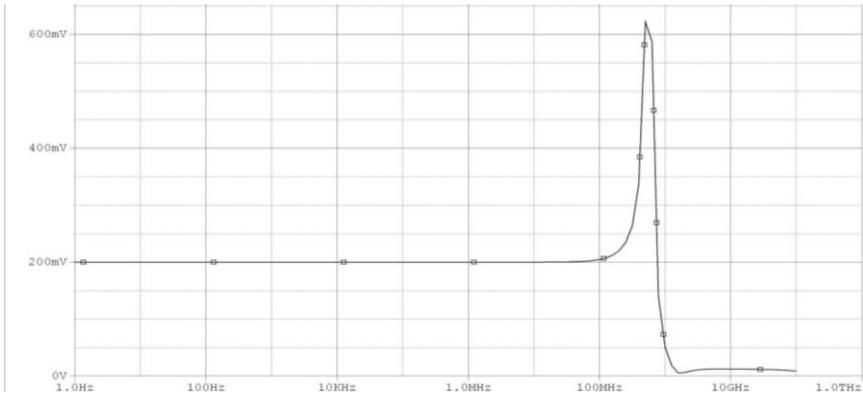
*+LIN V1 -0.3 0.3 0.1

.tran 0 10ms 1u

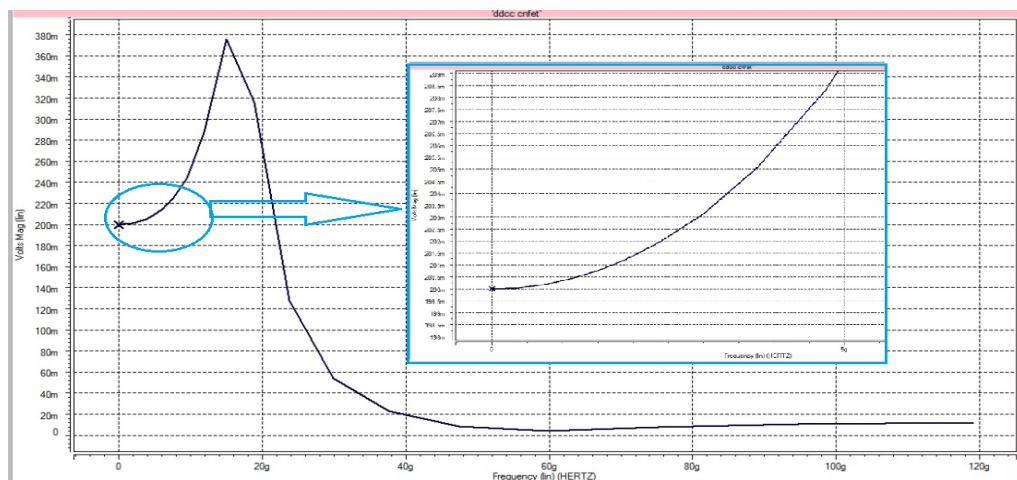
*.ac dec 10 1 100G

.probe

.end



(a)



(b)

Fig 6– AC characteristics of the DDCC (a) using MOS (350nm) technology having voltage consistency of 4.5% for 200mV, upto 100MHz and (b) using CNTFET having voltage consistency of 4.5% for 200mV, upto 5GHz.

In the fig-6 even though the response of the CNTFET based DDCC device doesn't have good high frequency response but upto 5 GHz it has a good voltage consistency comparitively the CMOS (350nm) technology.

IV. CIRCUIT REALIZATION OF PRECISION FULL-WAVE RECTIFIER

The full-wave rectifier circuit is shown fig- 7. This circuit uses only two DDCCs[4].The positive output voltage of the DDCC1 is connected to the negative output voltage of the DDCC2.

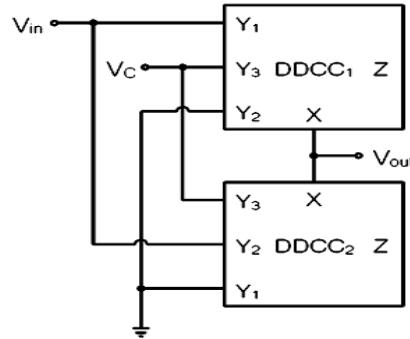


Fig.7. Full wave Rectifier circuit

The full-wave operation is as follows:

When $V_{in} > 0$, the voltage V_{in} is followed by the DDCC1 to the voltage V_{out} at X terminal while the DDCC2 is turn-off. In addition, when $V_{in} < 0$, the voltage V_{in} is followed by the DDCC2 to the voltage V_{out} at X terminal while the DDCC1 is cut-off .From the operation of the given full-wave rectifier explained.,the relations between the input voltage V_{in} , and the output voltage V_{out} , can be expressed as

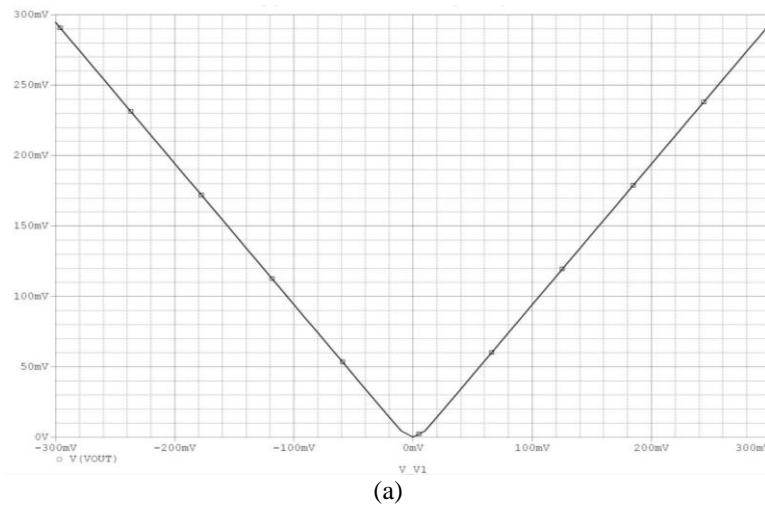
$$V_{in} > 0; V_{out} = V_{in} : \text{DDCC}_1 = \text{on}$$

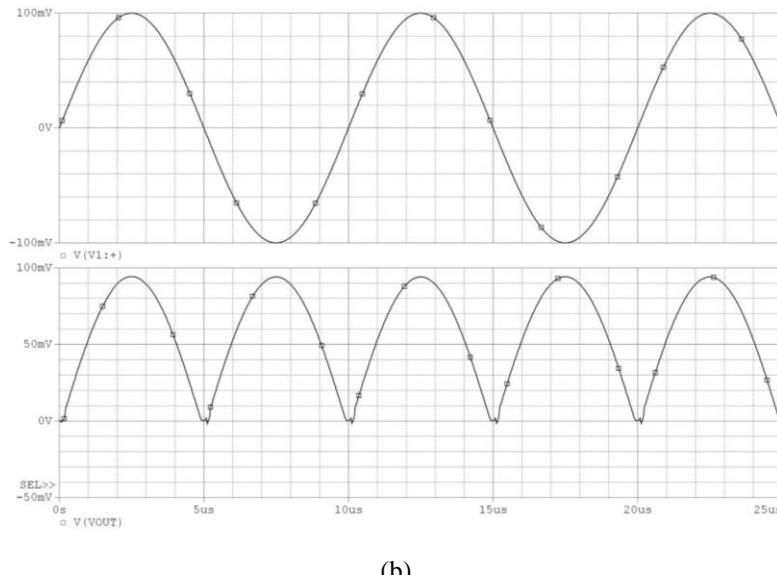
$$V_{in} < 0; V_{out} = -V_{in} : \text{DDCC}_2 = \text{on}$$

The complete output voltage of Fig.4 can be expressed as

$$V_{out} = |V_{in}|$$

Therefore, the given circuit provides the full-wave rectification[9]. V_c is auxiliary voltage. The circuit performance is shown in fig-8.





(b)

Fig. 8-precision full-wave rectifier response (a) and (b)

From above it is obvious that this rectifier can rectify any signal as low as 5 mv whereas for conventional rectifiers like full-wave rectifier[10][11] the minimum applied voltage should be above the Knee voltage of the semiconductor material being used (which is 0.7 V for silicon and 0.3v for germanium). This is a significant advantage of this circuit.

V. CONCLUSION

Realization of DDCC block is done with 50 times improved frequency response using carbon nanotube field effect transistor (single-walled-MOSFET like CNTFET). This DDCC has higher temperature stability, very high device density, high input impedance and low output impedance hence it easy to drive loads without using a buffering device. The implementation of precision full-wave amplifier has been successfully achieved. It can be applied in various non- linear analog signal processing circuits. The performance of the proposed circuit is confirmed from HSPICE simulation results. Since the CNTFET technology works on 0.9 Vdc drive voltage, the circuit is very power efficient.

REFERENCES

- [1] M. S. Dresselhaus, G. Dresselhaus, R. Saito "PHYSICS OF CARBON NANOTUBE"1995 Elsevier Science Ltd.
- [2] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon nanotube field effect transistors including non-idealities and its application—Part I: Model of the intrinsic channel region," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3186–3194, Dec. 2007.
- [3] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon nanotube field effect transistors including non-idealities and its application—Part II: Full device model and circuit performance benchmarking," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3195–3205, Dec. 2007.
- [4] Kumngern, M.; Saengthong, P.; Junnapiya, S. "DDCC-based full-wave rectifier" *5th International Colloquium on Signal Processing & Its Applications, 2009. CSPA 2009*.
- [5] B. Gilbert, "Translinear circuit: a proposed classification," *Electronics Letters*, vol. 11, pp. 14-16, 1975.
- [6] E. W. Greeneich, "Analog integrated circuit," *Chapman & Hall, New York, 1997*.
- [7] M. Kumngern and K. Dejhan, "DDCC-based quadrature oscillator with grounded capacitors and resistors," *Active and Passive Electronic Components*, vol. 2009, pp. 1-5, 2009, doi:10.1155/2009/987304.
- [8] Usa Tortechai, Montree Kumngern, Kobchai Dejhan "A CMOS Log-Antilog Current Multiplier/ Divider Circuit Using DDCC" *TENCON 2011 - 2011 IEEE Region 10 Conference*.
- [9] S. J. G. Gift, "A high-performance full-wave rectifier circuit" *International Journal of Electronics*, vol.89,pp.467-476,2000.
- [10] C.Toumazou, F. J. Lidgey, and S. Chatong, "High frequency current conveyor precision full-wave rectifier" *Electronics Letters*, vol.30,pp. 745-746,1994.
- [11] Z. Wang, "Full-wave precision rectification that is performed in current domain and very suitable for CMOS implementation" *IEEE Transactions on Circuits and systems-I*, vol.39, pp.456-462,1992.