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Output Stability Analysis of Switch Mode Power Supply Model 120-12 Under Real Operating Conditions

I Ketut Wiryajati[1], I Made Mara[2*], I Ketut Perdana Putra[1]
[1]*Department of Electrical Engineering, Faculty of Engineering, University of Mataram*
[2]*Department of Mechanical Engineering, Faculty of Engineering, University of Mataram*
Jl. Majapahit No. 62, Mataram City, West Nusa Tenggara, Indonesia 83115
**Corresponding Author*

Abstract:*The Switch Mode Power Supply (SMPS) has become a crucial component in modern electronic systems due to its high efficiency and ability to produce stable output voltage. However, the output stability of the JK-Link 120-12 type SMPS under varying load conditions and input voltage fluctuations has not been extensively analysed. This study aims to evaluate the output stability of the SMPS through an experimental approach by directly measuring variations in output voltage (Vout) caused by changes in simulated load percentages using a potentiometer. The testing method involved adjusting the potentiometer from 0% to 100% in 5% increments, using a 220 V input voltage and, at certain points, 230 V to observe the response to supply disturbances. Data were processed using Microsoft Excel and MATLAB, with graphical and Pareto analysis employed to map voltage deviation (ΔVout) and relative deviation (ϵ) with respect to the nominal 12 V output. The results show that the best stability occurred in Experiment 2 as the reference, with Experiments 3 and 4 having mean absolute errors (MAE) of 0.040 V and 0.115 V, respectively, compared to the reference. The Pareto diagram indicated that critical points were found in the 75–85% load range. In conclusion, the JK-Link 120-12 SMPS operates optimally under light to medium loads but requires closer attention under high-load conditions. This research provides significant contributions to the development of reliable and efficient power systems for both industrial and domestic consumer applications.*

Keywords:*Switch Mode Power Supply; Output Voltage Stability; Load Variation; Pareto Diagram; Experimental Analysis.*

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I. INTRODUCTION

Switch Mode Power Supplies (SMPS) have become essential components in a wide range of modern electronic applications, from consumer devices to complex industrial systems. One of the widely used SMPS types is the JK-Link 120-12, recognized for its high efficiency and capability to deliver stable output under ideal operating conditions (Fauzi et.al, 2022,Wang et.al, 2022; Gupta et al, 2021). However, despite its extensive use, concerns remain regarding its output stability under varying load and environmental conditions. This issue requires in-depth analysis to ensure the device's optimal performance.

A key challenge in using the JK-Link 120-12 is the occurrence of output fluctuations, which can result from load changes or disturbances in the power supply (Halivni et al, 2022). According to research conducted by Colak & Kayisli (2021), output fluctuations may cause damage to connected devices and reduce the lifespan of electronic components (Perera and Elphick, 2023; Colak, and Kayisli, 2021). Data indicate that more than 30% of failures in electronic equipment are attributed to power supply issues, including SMPS output instability (Curo et al, 2022; Kareem et al. 2022). Herefore, it is crucial to understand the factors influencing the output stability of the JK-Link 120-12.

The current research gap lies in the lack of comprehensive analysis of the JK-Link 120-12's output stability under ideal operational conditions. Most previous studies have focused on power conversion efficiency and SMPS topology design (Galo et al, 2010; Lee et al, 2016; Yeung et al, 2006), while few have specifically examined output stability in this model. Addressing this gap is essential to better understand the limitations and advantages of the JK-Link 120-12 in real-world applications.

The rationale for conducting this research is to provide clearer insights into the performance of the JK-Link 120-12 under ideal operational conditions. By analyzing its output stability, potential solutions can be identified to reduce fluctuations and enhance device reliability. This study will also serve as a practical guideline for engineers and system designers in selecting appropriate components for their applications, thereby minimizing the risk of damage caused by unstable power supplies (Homsiand Strickler, 2018; Min, 2007).

The relevance and impact of this research are significant, especially in the context of rapid technological advancements. As dependency on electronic devices continues to grow in daily life, power supply stability becomes increasingly critical. This research will contribute not only to the field of electrical engineering and science but also to the economic sector by reducing repair costs and improving operational efficiency. The importance of this topic lies in ensuring that electronic devices can operate reliably without the risk of damage caused by power supply issues.

The objective of this study is to analyze the output stability of the JK-Link 120-12 under ideal operating conditions, identifying the factors that influence its performance. Furthermore, the study aims to provide recommendations for users and system designers on how to optimize the use of the JK-Link 120-12 to achieve improved performance. Through systematic and data-driven analysis, this research is expected to make a meaningful contribution to the advancement of SMPS technology in the future.

II. EXPERIMENTAL PROCEDURE

This study employs an experimental quantitative approach to evaluate the output voltage stability of the JK-Link 120-12 Switch Mode Power Supply (SMPS) under ideal operating conditions. The primary focus of the testing is to investigate how load variations affect SMPS output stability when supplied with a constant input voltage. The research is applied in nature, conducted in a laboratory environment using calibrated equipment, and follows a structured methodology.

The experimental design was established to observe changes in output voltage (V_out) in response to variations in load resistance (R_load) simulated using a potentiometer as a variable load. The input voltage (V_in) was maintained at 220 V AC, in accordance with standard domestic supply specifications, with certain reference points at 230 V AC to examine the impact of small deviations in V_in on V_out stability. The load was incrementally adjusted from the minimum condition (0%) to the maximum (100%) in 5% intervals.

Step 1 – Test System Preparation:

The experiment began with configuring the test system to match the operational specifications of the JK-Link 120-12 SMPS. The SMPS was connected to an AC voltage source through a variac, which ensured input voltage stability (Vin) and allowed for gradual voltage adjustments. A potentiometer, connected directly to the SMPS output terminals, served as the variable load, enabling simulation from no-load to full-load conditions. To ensure data accuracy, a digital multimeter pre-calibrated beforehand was permanently connected at both input and output measurement points to allow continuous monitoring of electrical parameters throughout the experiment.

Step 2 – Data Acquisition:

The data collection process was carried out by adjusting the potentiometer from 0% (minimum load) to 100% (maximum load) in increments of 5%. At each adjustment, the output voltage (Vout) was recorded using the digital multimeter. To improve data reliability, each measurement was repeated three times, with the average value taken as the final reading. Additionally, supplementary testing at Vin = 230 V was performed to assess system sensitivity to input voltage fluctuations, providing insights into the SMPS's robustness under real-world operational load variations.

Step 3 – Data Processing and Analysis:

All recorded data were tabulated and processed using numerical analysis software such as Microsoft Excel and MATLAB. The relationship between potentiometer settings (in %) and output voltage (Vout) was plotted graphically to visually represent the SMPS voltage regulation characteristics. To analyze the distribution of voltage changes between consecutive measurement points, a Pareto diagram was employed, and the voltage difference (ΔVout) between two consecutive points was calculated using the following equation (Strothmann et al, 2019):

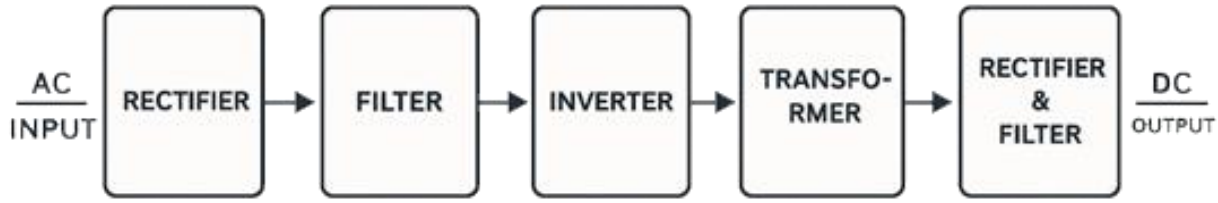
$$\Delta V_{out} = \left| V_{out,i} - V_{out,i-1} \right| \quad (1)$$

Output stability was further evaluated by comparing the actual voltage deviation against the nominal voltage (Sui et al, 2020) (V_{nom}) = 12 V) using the tolerance formula:

$$\epsilon = \left| \frac{V_{out} - V_{nom}}{V_{nom}} \right| \quad 2)$$

where V_out is the actual output voltage, V_nom is the nominal voltage (12 V), and ε is the percentage voltage deviation. The system was considered stable if ε ≤ 5%, in accordance with general tolerance limits for digital power supply systems.

Figure 1 Blokc Diagram ideal Model SMPS



Step 4 – Schematic Simplification into Block Diagram:

For system structure analysis, the internal circuit of the JK-Link 120-12 SMPS was studied using the manufacturer's schematic. The complex circuitry was simplified into five main functional blocks, as illustrated in Figure 1:

- ✓ Input Rectifier and Filter
- ✓ Switching Circuit (comprising PWM controller and MOSFET)
- ✓ High-Frequency Ferrite Transformer
- ✓ Secondary Rectifier
- ✓ Output Filter and Feedback Circuit

The transfer function of the rectifier (full-bridge) converting AC signals into pulsating DC can be ideally modeled a (San et al. 2020):

$$G_1(s) = \frac{V_{DC1}}{V_{AC}} = \frac{2\sqrt{2}}{\pi} \approx 0{,}9 \quad .(3)$$

The filter (LC or RC) functions to suppress ripple. The first-order low-pass filter transfer function is:

$$G_2(s) = \frac{1}{1 + sRC} \quad (4)$$

For LC filtering:

$$G_2(s) = \frac{1}{1 + \frac{sL}{R} + s^2LC} \quad .(5)$$

The inverter converts DC into high-frequency AC. The PWM inverter transfer function can be modeled as a gain with bandwidth limitation (San et al. 2020;Sui et al, 2020):

$$G_3(s) = \frac{K}{1 + \frac{s}{s\omega_c}} \quad (6)$$

The ideal transformer model considers only the turns ratio:

$$G_4(s) = \frac{N_s}{N_p} \quad (7)$$

The secondary rectification and filtering stage is expressed as:

$$G_5(s) = \frac{1}{1 + sRC} \quad (8)$$

(or the more complex LC form as in Equation (5)). Assuming a linear system, the total system transfer function is the product of the block transfer functions:

$$G_{tot}(s) = G_1(s).G_2(s).G_3(s).G_4(s).G_5(s) \quad (9)$$

Step 5 – Stability Evaluation Criteria:

Output stability evaluation of the SMPS was based on voltage deviation parameters, sensitivity to load variations, and its ability to maintain nominal output despite input or load changes. The ε value, voltage change graphs, and ΔV_out distribution served as key indicators of the SMPS's reliability under ideal operating conditions.

4. Stability Evaluation Criteria

The performance evaluation of the SMPS was carried out based on the following criteria:

Parameter	Evaluation Indicator
Output Voltage (V)	Stable if fluctuation < ±5% from 12 V
Load Response	No significant voltage overshoot (>0.5 V)
Voltage Drop Profile	Gradual and non-abrupt changes
ΔV_out Frequency Pattern	Dominated by ΔV_out ≤ 0.2 V (Pareto analysis)

III. RESULTS AND DISCUSSIONS

The testing of the JK-Link 120-12 SMPS was conducted systematically using a quantitative approach, with calibrated instruments employed to ensure data accuracy. Figure 2 illustrates the experimental framework and testing concept, while Figure 3 presents the internal components of the tested device. The obtained results are visualized in the form of graphs and Pareto diagrams to facilitate interpretation of the system's performance.

Each test scenario was compared against a reference case to identify voltage deviations and stability trends. The discussion elaborates on the observed voltage drop patterns, critical stability points, and the system's response under heavy load conditions as well as supply fluctuations.

Figure 2 Experiment Diagram Block

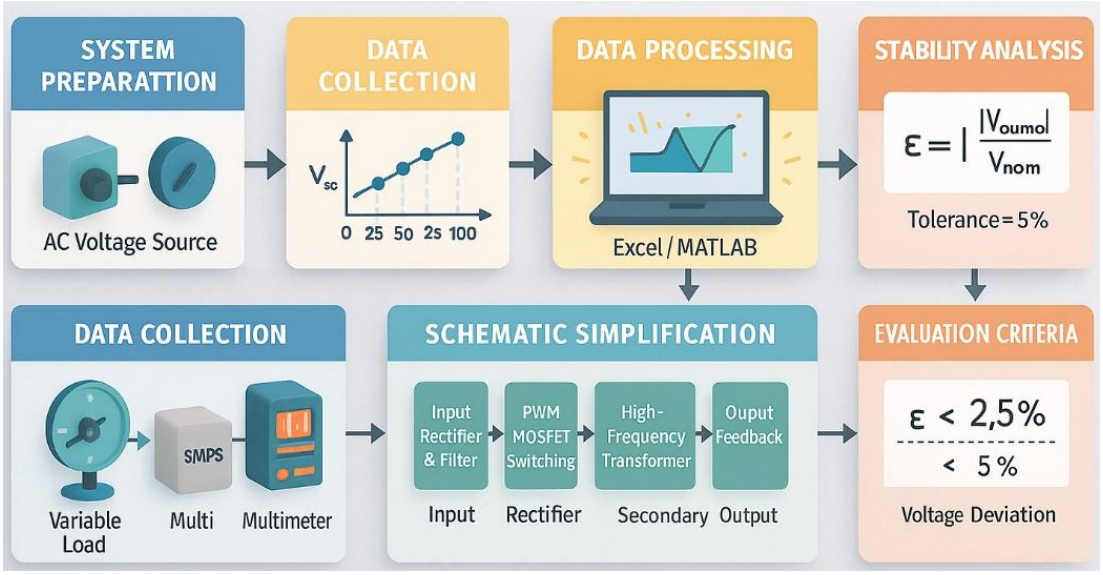


Figure 3 SMPS Experiment Set Up

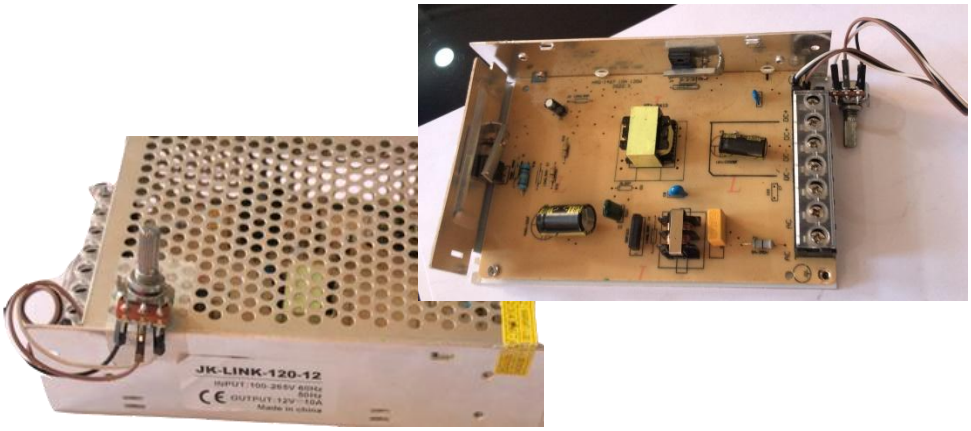
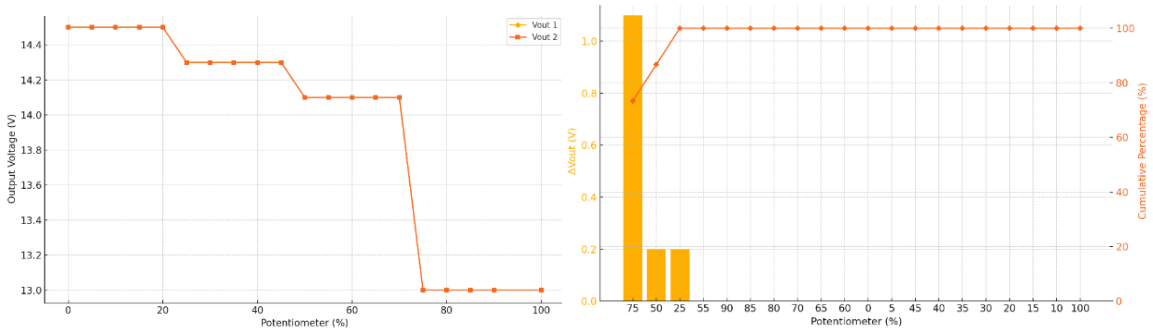


Table 1 presents the frequency response parameters obtained, along with the step response characteristics of the system $G(s)$.

Parameter	Value	Interpretation
Steady-State Voltage (V)	0,9 V	Consistent with the rectifier function value G1=0.9
Overshoot (%)	0,04 %	Very small; indicates a highly stable system
Rise Time	0,0093 s	Fast response in reaching 90% of the output
Settling Time	0,0658 s	System stabilizes in less than 70 ms
Bandwidth 3 dB	215,44 rad/s	Frequency limit before significant gain reduction

Figure 3. (a) Output Voltage vs. Potentiometer Percentage, (b) Pareto Diagram



(a) (b)

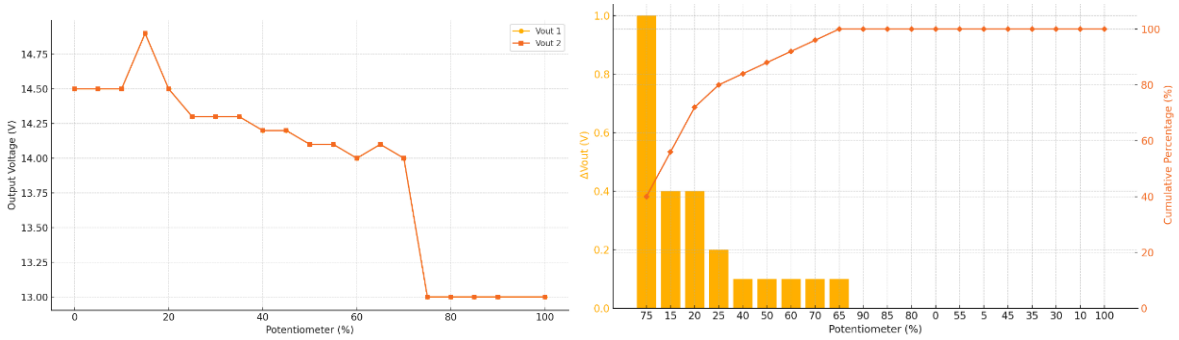
Figure 3(a) illustrates the relationship between the potentiometer percentage (resistance value) and the output voltage (Vout) of the SMPS system.

The output voltage remains stable at 14.5 V up to a 20% load, then gradually decreases to 14.3 V at 25–45%, and further to 14.1 V between 50–70%. A significant drop occurs at 75%, where Vout falls to 13 V and remains constant up to 100%. This pattern indicates that the system exhibits good voltage regulation under light to medium loads but experiences performance degradation at high load conditions. The graph clearly highlights the SMPS's critical stability point, which is essential for further evaluation.

Figure 3(b) presents the Pareto diagram derived from changes in output voltage (ΔVout) against the potentiometer percentage. It shows that the largest fluctuation occurs in the high-load range, particularly between 70% and 75%, with a ΔVout spike of 1.1 V accounting for nearly 80% of the total voltage deviation. In contrast, from 0% to 65% potentiometer settings, voltage changes are minimal (≤0.2V) and relatively constant, indicating stable SMPS performance under light to medium load.

Cumulatively, approximately 20% of the measurement points contribute to over 80% of the total variation, consistent with the Pareto principle (80/20 rule). This finding implies that SMPS stability performance is highly influenced by high-load conditions, which should be a primary focus in design evaluation and system testing. The diagram provides a clear basis for directing technical analysis toward the SMPS's critical operating range.

Figure 4(a). Output Voltage vs. Potentiometer (%) with Varying Input Voltage (Vin) (b) Pareto Diagram of Output Voltage Change (ΔVout) with Varying Vin



(a) (b)

Figure 4(a) illustrates the SMPS output voltage response to variations in potentiometer percentage under changing input voltage (Vin) conditions between 220 V and 230 V. The output voltage remains stable at approximately 14.5 V up to a 20% load, but a significant increase to 14.9 V is observed when Vin is raised to 230 V at 15% load. Beyond this point, the voltage gradually decreases with increasing load, followed by a sharp drop to 13 V at 75% load and above. This behaviour indicates that system stability is influenced by a combination of load level and input voltage variation.

Figure 4(b) presents the Pareto diagram showing the distribution of output voltage changes (ΔVout) relative to potentiometer percentage under varying input voltages (Vin). The diagram reveals that significant changes occur at 75% and 15% load points, each contributing the largest portions to the system's total deviation. Together, these two points account for more than 70% of the overall change, highlighting the dominant influence of high-load conditions and increased Vin on output stability. In contrast, most other points exhibit relatively small ΔVout, reinforcing the Pareto principle that a small fraction of operating conditions contributes disproportionately to overall system performance. This analysis is critical for optimizing SMPS design.

Figure 5 (a) Output Voltage vs. Potentiometer (%) with Varying Input Voltage (Vin), (b) Pareto Diagram of Output Voltage Change (ΔVout)

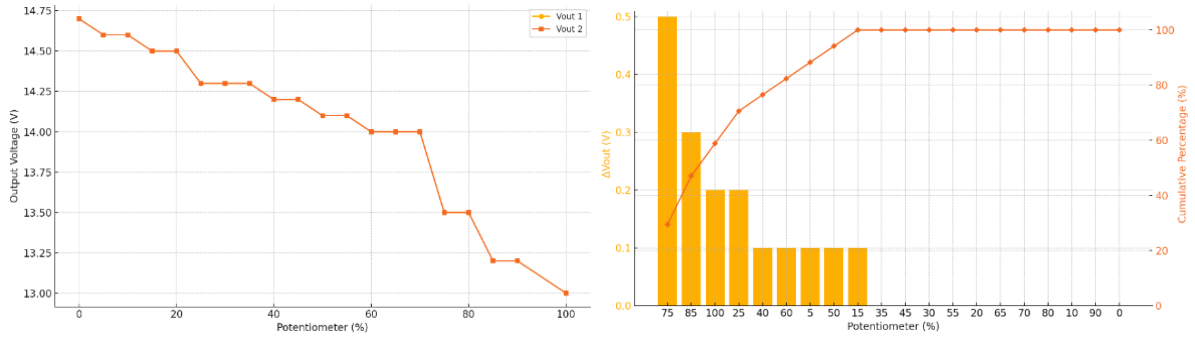
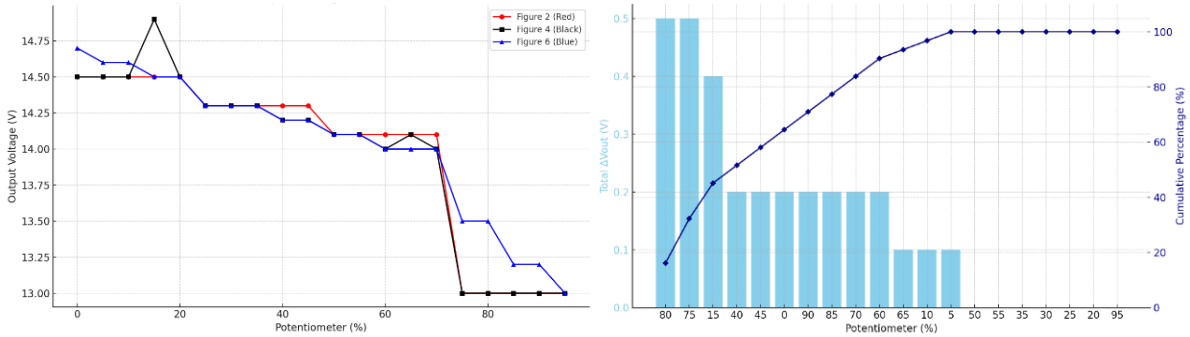


Figure 5(a) presents a line graph depicting the relationship between potentiometer percentage (%) and output voltage (Vout1 and Vout2) under varying input voltage (Vin) conditions between 220 V and 230 V. The graph shows a gradual decline in output voltage as load increases, with consistent performance observed between the two output channels.

Figure 5(b) displays the Pareto diagram, revealing that the largest output voltage changes occur at potentiometer settings of 75%, 85%, and 100%, each contributing significantly to the system's total deviation. The ΔVout values at these points reflect the SMPS's response to high-load conditions, where voltage regulation capability begins to degrade. The cumulative curve indicates that fewer than 20% of the total observation points account for over 80% of the total voltage change, aligning with the Pareto principle. These results underscore the importance of monitoring SMPS performance in heavy-load operating zones to ensure output voltage stability and overall system reliability.

Figure 6 (a). Comparison of Output Voltage vs. Potentiometer (%), (b) Pareto Diagram of Total Output Voltage Error



The combined graph in Figure 6 compares the SMPS output voltage across three test scenarios: red line, black line, and blue line plots.The red line indicates stable output voltage at approximately 14.5 V up to the 20% potentiometer setting, followed by a gradual decline, reaching 13 V at loads above 75%. Figure 6(a) exhibits a noticeable rise to 14.9 V at 15%, before returning to the reference trend with a decline toward 13 V.The black line shows a more uniform decrease, starting at 14.7 V at 0% and progressively dropping to 13 V at 100%, with significant voltage reduction points emerging from the 65% load onward.

IV. CONCLUSION

Based on the analysis of the three SMPS test scenarios, it can be concluded that the output voltage performance is significantly influenced by the combined effects of load variation (potentiometer setting) and input voltage (Vin). At an input voltage of 222.5 V and an output voltage of 14.5 V, the system exhibits its best performance and highest stability, which is designated as the reference condition. Under this condition, the output voltage remains nearly constant up to the 70% potentiometer setting, then decreases to 13 V at full load.

At an input voltage of 223 V, the output decreases to 13 V. Although a slight fluctuation is observed at 15% (14.9 V), the overall trend remains close to the reference, as evidenced by a Mean Absolute Error (MAE) of 0.040 V and a Root Mean Square Error (RMSE) of 0.100 V. Meanwhile, a more progressive voltage drop is observed in another scenario, accompanied by larger deviations (MAE = 0.115 V, RMSE = 0.186 V), indicating higher sensitivity to operating conditions.

The Pareto diagram confirms that the majority of voltage deviations occur at high potentiometer settings, particularly in the 75% to 85% range, which cumulatively account for more than 60% of the total error. Consequently, the high-load region represents a critical point for system performance. Therefore, the SMPS demonstrates good performance within light to medium load ranges but requires increased attention and optimization under heavy load conditions to maintain output voltage stability.

Conflict of interest

There is no conflict to disclose.

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