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Design Of Logic Blocks With Increased Efficiency For FPGA

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Abstract: *This paper presents different possibilities of configurable logic block (CLB) a hybrid cluster composed of look up table (LUTs) and universal logic gates (ULGs). A ULG is designed to realize logical functions with better efficiency compared to that of LUT based design. Pure LUT based architecture incurs a longer delay or doubles the area compared to the ULG based design. Since ULG is not capable of implementing all the classes of logic functions, a hybrid CLB that contains a mixture of LUTs and ULGs is the solution to address the generality problem and to achieve the benefits in the case of area, performance, and power. The power analyses the effect of different combinations of LUTs and ULGs in one basic logic element (BLE).The results show that, compared to pure LUT design, the experimented architecture design saves up to 17.1% logic power,52% time and 4.5% logic area.*

Keywords: *FPGA, logic element, ULG, LUT, logic block, VTR.*

I. Introduction

The field programmable gate array (FPGA) devices are made of an array of logic blocks connected through programmable interconnects and input / output blocks (I/o blocks).The programmable nature of the logic block allows bit to be a reprogrammed for different applications and functionalities. It can be configured by the user after manufacturing. The FPGA vendors provide high flexibility in its configuration by exploiting the potential of the logic blocks and its connectivity.

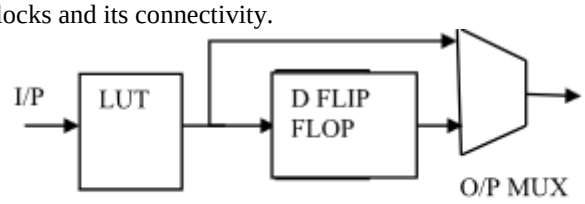

Fig. 1 Basic Logic element

The programmable logic blocks are termed as configurable logic Blocks (CLB). A cluster of Basic Logic Elements (BLE) in turn makes up the CLB, interconnected through programmable routing network. The BLEs, in turn, has a function generator, flip flop and multiplexer. The logic block structure forms the very basis for the speed and the density of the FPGA .The most commonly used function generator look up the tables K input looks up table that is a digital memory with 2^k bits, k address line ,one output line. The truth table of the logic function is stored in the correct address of the memory and k address lines are the input that allows the implementation of the truth table. The d flip flop permits the implementation of the combinational function .The multiplexer combines the output of the LUT and the d flip flop produce the logic block output. A logic block thus performs both combinational and sequential function. The LUTs that are most preferred in the logic block can cause area over head and redundancy. This is because, among the 2^2n the function that are implemented by configuring the 2^n configuration bits of the LUT, only a few function are frequently used. So a lot of LUTs remains unused and its causes wastages of area [3].So to overcome this disadvantage there is a need for alternate solution and universal logic gate comes to the scenario. Implementing a universal logic gate based hybrid logic element that realize the most commonly used function in the MCNC bench mark circuits, the reduction of the LUTs leads to lower power consumption[8].

Jonathan rose et.al.[5] have explained the various programming technology used in the FPGA like the SRAM, anti –fuse and EEPROM technology. They have discussed the effect of the logic block characteristics and is concluded by drafting the ideology the grouping more logic into a block and reducing a amount of slow wiring improves the speed and area efficiency of the FPGA.

SatwantSingh et.al [7], have discussed the various logic block implementation using NAND gate logic, LUT, MUX logic, and AND-OR gates logic and compare all of these with a different number of input. The results state that logic block made of 2 input NAND gate produce the worst delay, 5/6 input LUTs shows the lowest delay, 5/6 input multiplexer logic shows higher delay than LUT.AND- OR gates produce a delay in the range between LUTs and MUX.The paper also showcase the various steps involved in the logic synthesis.

Vaughn Betz and Jonathan rose [9] have discussed clustering of logic blocks and its effects on FPGA performance.LUT with more number of inputs can implement more logic with fewer logic blocks and save routing area, but its complex and becomes impractical for implementation. So instead several logic blocks can be interconnected together using local routing .The basic logic elements(BLE) consisting of the LUT, flip-flop, and mux, are thus packed together with common inputs and allows local reuse of generated outputs using crossbars. In spite of the requirement of 4N BLE inputs (N- no. of LUTs), mere 2N+2 inputs(50-60% of the total input pin count) are sufficient for the cluster to achieve 98% logic optimization[4].

In this paper, a ULG structure [2] composed of four 2input NAND gates, three configurable inverters and multiplexers are used, which realizes the NPN classes discussed in section II.The implementation of a hybrid logic element (HLE) using ULG structure, followed by the FPGA architecture implementation using HLEs and BLEs are explained in the same section. Section III showcases the results obtained from the design and the further discussions related to it. Section IV drafts the conclusions and the future scope of the work.

II. Background and Concepts

A. NPN Equivalence:

The design of ULG[8] adopts the concept of NPN equivalence to overcome the disadvantage of LUT. According to the concept , two functions are said to be NPN equivalent when one function can be obtained from the other by permuting the inputs are negating input are output of the function. By doing so, it can cover up to(2^N+1,N!) distinct function.

RANK	REPRESENTATIVE FUNCTION OF THE NPN CLASS	APPEARANCE RATIO(%)
1	ABCD	22.618
2	A(B+C+D)	21.205
3	A(B+CD)	19.211
4	AB+CD	11.06
5	(A+B)CD	5.775
6	OTHERS	20.13

Table. 1 NPN classes and their appearance ratio in the MCNC circuits

So by using NPN equivalence, 80% of the frequently used functions in the MCNC golden 20 bench mark circuits can be grouped under five classes are namely:[ABCD], [AB+CD],[A(B+CD)],[A(B+C+D)]and [(A+B)CD].Designing a logic block that implements these five classes of functions can save a lot of area.

B. Universal Logic Gates :

Implements the five classes of function grouped using NPN equivalence. The ULG structure is made of four NAND gates, 3 configurable inverters, and one multiplexer. The ULG can implement the 5 NPN classes by configuring the corresponding configurable inverters and multiplexer 2 different modes.

Table 2 shows the configuration changes to be done to the 3 configurable inverters and the multiplexer to implement the 5 functions using the universal logic gates. The ULG only has 4 configurable bits. Compared this with 16 configurations bits of a conventional LUTs can produced dramatic area and power reduction.

Fig. 2 Universal Logic Gate

Logic function	Config INV1	Config INV1	Config INV1	Gate with '1' as input
ABCD	Inverter	inverter	buffer	NAND
(A+B)CD	inverter	buffer	buffer	NAND
AB+CD	buffer	buffer	inverter	NAND
A(B+CD)	buffer	buffer	inverter	NAND
A(B+C+D)	inverter	buffer	inverter	NAND
ABCD	Inverter	inverter	buffer	NAND

Table. 2 Configurations For The Five Functions

III. Proposed Hybrid Logic Blocks

A. Hybrid Logic Element:

The hybrid logic element[HLE] shown in figure is a basic logic element with a ULG in the place of LUT HLEs are used in combination with BLEs in the CLB to get the maximum efficiency out of the CLB.

Similar to the BLE, the ULG output is given to the multiplexer separately and through a D flip flop. The straight connection accounts to the sequential operation and the connection through the D flip flop accounts to the combinational operations.

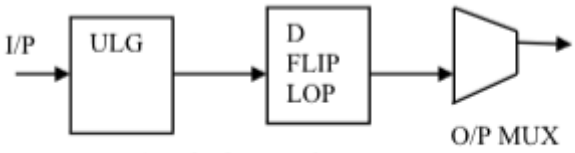

Fig.3. Hybrid Logic element

B. Proposed Logic Block:

Logic blocks are constructed by the combining the BLEs and HLEs in different ratios and their performance are analyzed which are discussed in the next section .Among the various proposed blocks, the combination of one BLE with 6 –LUT, two BLEs with 5-LUT and 5-HLEs shown in figure is observed to be most efficient logic blocks cluster the HLEs integrate the implementation of the functions that are grouped under the 5 classes using NPN equivalence. The rest of the functions are supposed to be implemented through the BLEs.

The crossbar has many multiplexers in it .The number of multiplexer is equivalent to the number of inputs of the logic block each multiplexer takes into it the external input and the feedback output as its input and selects anyone of it to be the output. So the selected line is given as an input to the logic element. This implies that the four inputs of the LUT in a logic element is obtained from four multiplexers in the crossbar.

IV. Results

A. Analysis Methodology:

Firstly universal logic gates[ULG] are to be constructed using the basic gates and analyzed by comparing it with LUTs of a different number of inputs than hybrid logic element is to be constructed using the ULG and analyzed by comparing with various BLEs composed of LUTs of a different number of inputs finally, logic cluster are to be made using different combination of BLEs and HLEs. The clusters that provide that best performance results are concluded to the most efficient configurable logic blocks.

B. CADENCE:

Cadence allows all the stage of IC design and verification to be done in a single environment. So the newly build logic block is evaluated using cadence .It is essential to evaluate a logic blocks because the performance of a single block reflects on a larger scale in a complete FPGA architecture which will include several such blocks. So the newly created logic block is evaluated for its performance and it is compared with a conventional design.

Initially ,the basic component inside the logic element is designed in cadence.LUTs of a different number of inputs 4,5and 6 inputs LUTs are created and compared to analyze the performance of the components have been studied on the basis of area gates leakage power dynamic power, worst case delay.

Element	Area(NM)	gates	Leakage power (nw)	Dynamic power (nw)	Total power (nw)	Worst case delay (ps)
4-LUT	238	60	1584.833	7581.659	9166.492	132
5-LUT	70	124	271.465	1376.927	1648.392	12
6-LUT	143	252	551.689	2798.271	3349.958	12
ULG	19	7	63.428	379.547	442.975	63

From the table 3,its found that area, gates, and power of ULG are very much lower when compare to 4,5 and 6 input LUTs. the worst case delay values range in between that of 4 input LUTs and 5 and 6 input LUTs. Compared to 4 –LUT, the performance of 5 and 6 input LUTs are better in terms of all the parameter.

C. Evalution Of Basic Logic Element

Logic element are constructed using the so formed components .the logic elements formed are namely :

- BLE with 4-LUT, flip –flop, and mux
- BLE with 5-LUT, flip-flop, and mux

- BLE with 6-LUT, flip-flop, mux
- HLE with ULG

The logic element are implemented and the performance of the above elements are the compared and depicted in table IV

Table IV: Performance Analyses Of Various Logic Elements

Logic element	Area (nm)	gates	Leakage power (nw)	Dynamic power (nw)	Total power (nw)	Worst case delay (Ps)
BLE with 4-LUT	270	65	1789.373	11214.899	13004.272	145
BLE with 5-LUT	89	129	372.367	3159.750	3532.117	298
BLE with 6-LUT	161	257	652.589	4581.094	5233.683	298
HLE with ULG	51	12	267.969	2494.876	2762.845	323

The 4 different logic elements are constructed and it is observed IV, that the BLE with 5-LUT shows result in the range between that of BLEs with 4 and 6 inputs LUT. HLE with ULG shows better result than the other three and is, therefore, more desirable than the BLEs.

D. Evaluation Of Logic Clusters

Finally, clusters are designed using so formed logic elements. Various combination are analyzed and compared and the once with the best results are put down as follows:

The cluster analyzed is

a) Four BLEs of 6-LUT and 4 HLEs
b) Three BLEs of 6-LUT, two BLEs of 5-LUT and three HLEs
c) Three BLEs of 6-LUT, five HLE
d) Two BLEs of 6-LUT, two BLEs of 5-LUT and 4 HLEs
e) Two BLEs of 6-LUT, one BLE of 5-LUT and five HLEs
f) One BLEs of 6-LUT, two BLE of 5-LUT and five HLEs

These clusters are compared with the conventional cluster with ten BLEs of 4-LUT and the one proposed in [8] with four BLEs of 4-LUT of six HLEs. The result is shown in table V.

V. Conclusion

Different possibilities of configurable logic block (CLB) a hybrid cluster composed of look up table (LUTs) and universal logic gates (ULGs). A ULG is designed to realize logical functions with better efficiency compared to that of LUT based design. Pure LUT based architecture incurs a longer delay or doubles the area compared to the ULG based design. Since ULG is not capable of implementing all the classes of logic functions, a hybrid CLB that contains a mixture of LUTs and ULGs is the solution to address the generality problem and to achieve the benefits in the case of area, performance, and power. The power analyses the effect of different combinations of LUTs and ULGs in one basic logic element (BLE).The results show that, compared to pure LUT design, the experimented architecture design saves up to 17.1% logic power,52% time and 4.5% logic area.

References

[1]. Tsung-Han Yu , Chia-Hsiang Yang , Cabric.D , Markovic. D,"A 7.4-mW 200-MS/s Wideband Spectrum Sensing Digital Baseband Processor for Cognitive Radios" IEEE Journal of Solid-State Circuits, Vol.47, no.9, pp.2235-2245, 2012.

[2]. Oude-Alink, M.S , Klumperink, E.A.M , Kokkeler, A.B.J, Wei Cheng , Zhiyu Ru , Ghaffari, A, Wienk, G.J.M, Nauta, B, "A CMOS spectrum analyzer frontend for cognitive radio achieving +25dBm IIP3 and −169 dBm/Hz DANL", IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp.35-38,2012 .

[3]. Oude Alink. M.S, Klumperink.E.A.M, Kokkeler. A.B.J, Soer. M.C.M,Smit.G.J.M, and Nauta, B "A CMOS-Compatible Spectrum Analyzer for Cognitive Radio Exploiting Cross correlation to Improve Linearity and Noise Performance", , IEEE Trans. on Circuits and Systems- I ,vol-59,no.3,pp.479-492.Jun 2012.

[4]. Mahrof. D.H,Klumperink. E.A.M, Haartsen.J.C,and Nauta. B. "On the Effect of Spectral Location of Interferers on Linearity Requirements for Wideband Cognitive Radio Receivers" IEEE Symposium on New Frontiers in Dynamic Spectrum, pp.1-9, 2010.

[5]. N. A. Moseley, E. A. M. Klumperink, and B. Nauta, "A spectrum sensing technique for cognitive radios in the presence of harmonic images," in Proc. 3rd IEEE Symp. New Frontiers Dyn. Spectrum Access Netw. (DySPAN),

2008, pp. 1–10..

[6]. D. Cabric, A. Tkachenko, and R. W. Brodersen, "Spectrum sensing measurements of pilot, energy, and collaborative detection," in Proc. IEEE Mil Comm. Conf. (MILCOM), 2006, pp. 1–7.

[7]. Mitola. J, Maguire.G.Q,"Cognitive radio: making software radios more personal" IEEE Personal Communications, vol.6,no.4, pp.13-18,1999