Circuit for Square Root of Multiplication

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ABSTRACT: A circuit which accepts two input dc voltages \( V_1, V_2 \) and produces an output voltage \( V_O = \sqrt{V_1V_2} \) by using double dual slope principle with op-amps and analog switches is described in this paper. Verification of the feasibility of the circuit is established by way of test results on a prototype.

KEY WORDS: Integrator, flip flop, comparator, transistor switch and peak detector

I. INTRODUCTION

Square rooters find applications in many measurement and instrumentation system. Few examples are (i) Phase sensitive detector and (ii) Impedance measurement. The author Selvam proposed few square rooters by using (i) double dual slope integrators, double control amplifiers, one comparator and one peak detector [1] (ii) a saw tooth generator, comparator, switch and two op-amps [2] and (iii) a square rooter in which a multiplier is used in the feedback path of an operational amplifier (OP-AMP) [3]. There are several other square rooting circuits. (i) Rievuraja and Kamsri realised a technique [4] by use of the op-amp supply current sensing which utilises an inherently quadratic characteristic of the op-amp class –AB output stage. (ii) Rievuraja proposed a square rooter [5] using operational transconductance amplifiers (OTAs) as the only active elements. (iii) Filanovsky and Balkes proposed a square rooter [6] by using an opamp and two nested transistors. One of these transistors is in pinch – off and the other in the triode region of operation. (iv) Liu’s square rooter [7] in which second generation current conveyors is used as high performance active building block. A further extension of square rooter circuit is the square root of multiplication of two voltages. Double dual slope multiplier – cum- divider circuit proposed by the author in [8] is reformatted to function as square rooting of multiplication and is explained in this letter.

II. CIRCUIT ANALYSIS

The proposed circuit diagram is shown in the Fig. 1. Let initially, the SR flip flop output be LOW (\(-V_{CC}\)). The transistor \( Q_1 \) is OFF, control amplifier \( OA_1 \) will work as non-inverting amplifier and hence the integrator \( OA_2 \) output will be

\[
V_p = \frac{1}{r_1C_1} \int_0^t [V_{O} + V_p(t)] dt = \frac{V_O}{r_1C_1}(1 + V_p(t)) \tag{1}
\]

When the output of the integrator \( OA_2 \) exceeds the second input voltage \( V_1 \), say at time \( t_1 \), the SR flip flop is set to HIGH (\(+V_{CC}\)) by comparator \( OA_3 \). The transistor \( Q_1 \) is ON, control amplifier \( OA_1 \) will work as inverting amplifier and hence the integrator output will then be
When the output of the integrator exceeds the second input voltage \(-V_1\), say at time \(t_1+t_2\), the RS flip flop is reset to LOW by the comparator \(O A_4\) and the cycle repeats. The associated waveforms generated under steady state operation are shown in Fig. 2, where \(V_p(0)\) is taken as \(-V_1\). From equation (1) and referring to fig we have

\[ V_{p} = \frac{1}{R_1 C_1} \int_{t_1}^{t_2} -V_{O} \cdot d \cdot t + V_{p}(0) \cdot \cdot \cdot + \cdot V_{p}(t-t_1) + V_{p}(0) \]  

(2)

Under steady state condition, \(t_1 = t_2 = T/2\) and at \(t\), \(V_p = 2V_1\) and hence

\[ 2V_1 = \frac{V_O}{R_1 C_1} \cdot \frac{T}{2} \]  

(3)

\[ T = \frac{4V_1 R_1 C_1}{V_O} \]  

(4)
The ON time of the square waveform $V_0$ at the output of SR Flip Flop shorts the non-inverting terminal of op-amp $OA_4$ to GND through the transistor $Q_2$. The amplifier $OA_5$ will work as inverter and $V_2$ is connected to the integrator $OA_6$. Its output $V_K$ will be

$$V_K = \frac{1}{R_2C_2} \int_V^0 V_2dt = -\frac{V_2}{R_2C_2} \tag{5}$$

The OFF time of $V_0$ will enable the amplifier $OA_5$ to work as non-inverting amplifier and hence $-V_2$ will be given to the integrator $OA_6$. Then its output will be

$$V_K = \frac{1}{R_2C_2} \int_V^0 V_2dt = -\frac{V_2}{R_2C_2} \tag{6}$$

Another triangular wave of peak to peak value of $\pm V_O$ is generated at the output of $OA_6$. From Equation (6) and waveforms in Fig. 2, the fact that at $t=T/2$, $V_K = 2V_0$

$$2V_0 = \frac{V_2}{R_2C_2} \tag{7}$$

$$V_O = \frac{V_1V_2}{V_O} \frac{R_1C_1}{R_2C_2} \tag{8}$$

If $R_1C_1 = R_2C_2$, then

$$V_O^2 = V_1V_2 \tag{9}$$

$$V_O = \sqrt{V_1V_2} \tag{10}$$

III. EXPERIMENTAL RESULTS AND CONCLUSION

The proposed circuit is tested in our laboratory. LF 356 ICs are used for all op-amps. IC 4027 is used for SR Flip Flop. Conventional peak detector circuit using op-amp is used. A power supply of $\pm V_{CC} = \pm 7.5V$ is chosen. The test results are shown in graphs of Fig. 3 and Fig. 4. A new circuit for square rooting of multiplication is described. The polarity of all input voltages must be single polarity only. Hence the proposed circuit is of single quadrant type.

Fig. 3 Test results for constant $V_2 = 2V$
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REFERENCES


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